## Claims

What is claimed:

1. An apparatus for writing to memory cells comprising:

   a write current generator for generating a write current that is coupled to an array of memory cells;

   a threshold detector for feeding back a control indicator to the write current generator if the write current is one of greater than a maximum write current threshold or less than a minimum write current threshold.

2. The apparatus of claim 1, wherein the threshold detector determines whether the write current is greater than a maximum write current threshold or less than a minimum write current threshold by summing a write current offset to the write current, and determining whether a write error occurs.

3. The apparatus of claim 2, wherein the write current offset increases the write current to determine whether a magnitude of the write current should be decreased.

4. The apparatus of claim 2, wherein the write current offset decreases the write current to determine whether a magnitude of the write current should be increased.

5. A method for regulating a magnetic memory cell write current, comprising:

   modifying a magnetic memory cell write current by summing a write current offset to the magnetic memory cell write current;

   determining whether writing to a magnetic memory cell with the modified magnetic memory cell write current results in a write error condition;

   if a write error condition exists, then incrementing the magnetic memory cell write current, or decrementing the magnetic memory cell write current, until the write error condition is eliminated.

6. The method for regulating a magnetic memory cell write current of claim 5, wherein the write current offset decreases the magnetic memory cell write current to determine whether a magnitude of the magnetic memory cell write current should be increased.

7. The method for regulating a magnetic memory cell write current of claim 5, wherein the write current offset increases the magnetic memory cell write current to determine whether a magnitude of the magnetic memory cell write current should be decreased.

8. The method for regulating a magnetic memory cell write current of claim 5, wherein the magnetic memory cell write current comprises an easy axis current and a hard axis current, the hard axis current being set to a default value, and the easy axis current being incremented.

9. The method for regulating a magnetic memory cell write current of claim 6, wherein the magnitude of the magnetic memory cell write current is increased by incrementing an up/down counter.

10. The method for regulating a magnetic memory cell write current of claim 7, wherein the magnitude of the magnetic memory cell write current is decreased by decrementing an up/down counter.

11. The method for regulating a write current for a magnetic memory cell of claim 7, wherein the magnetic memory cell write current comprises an easy axis current and a hard axis current, the hard axis current being zeroed, and the easy axis current being decremented.

12. The method for regulating a magnetic memory cell write current of claim 9, the up/down counter is connected to a current digital to analog converter (iDAC) that generates the magnetic memory cell write current.

13. The method for regulating a magnetic memory cell write current of claim 12, wherein the write current offset is subtracted from the magnetic memory cell write current by subtracting a current offset from a current reference of iDAC.

14. The method for regulating a magnetic memory cell write current of claim 13, wherein the current offset is subtracted from a current reference of iDAC by selecting which transistors of a plurality of transistor are connected in parallel in a current mirror, wherein the current mirror generates the current reference.

15. The method for regulating a magnetic memory cell write current of claim 14, the up/down counter is connected to a current digital to analog converter (iDAC) that generates the magnetic memory cell write current.

16. The method for regulating a magnetic memory cell write current of claim 15, wherein the write current offset is added to the magnetic memory cell write current by adding a current offset to a current reference of iDAC.

17. The method for regulating a write current for a magnetic memory cell of claim 16, wherein the current offset is added to a current reference of iDAC by selecting which transistors of a plurality of transistor are connected in parallel in a current mirror, wherein the current mirror generates the current reference.

18. An magnetic random access memory (MRAM) array comprising:

an MRAM cell;

a write current generator for generating a MRAM cell write current for writing to the MRAM cell; and

a write current monitor for maintaining a magnitude of the write current within a minimal write error range.

19. The MRAM array of claim 18, wherein the write current monitor maintains the magnitude of the write current within the minimal write error range by summing a

write current offset to the write current, determining whether a write error occurs, and incrementing or decrementing the write current until the error condition is eliminated.

20. The MRAM array of claim 19, wherein the write current offset increases the write current to determine whether a magnitude of the write current should be decreased.

21. The MRAM array of claim 19, wherein the write current offset decreases the write current to determine whether a magnitude of the write current should be increased.

22. The MRAM array of claim 20, wherein the magnitude of the write current is increased by incrementing an up/down counter.

23. The MRAM array of claim 21, wherein the magnitude of the write current is decreased by decrementing an up/down counter.

24. A method for regulating a write current for a magnetic memory cell, comprising:

modifying a magnetic memory cell write current by adding a write current offset to the magnetic memory cell write current;

applying the modified magnetic memory cell write current to a test magnetic memory cell;

testing the test magnetic memory cell for a write error condition;

if a write error condition exists, then incrementing the magnetic memory cell write current, or decrementing the magnetic memory cell write current, until the write error condition no longer exists.

25. The method for regulating a write current for a magnetic memory cell of claim 24, wherein the write current offset decreases the magnetic memory cell write current to determine whether a magnitude of the magnetic memory cell write current should be increased.

26. The method for regulating a write current for a magnetic memory cell of claim 24, wherein the write current offset increases the magnetic memory cell write current to determine whether a magnitude of the magnetic memory cell write current should be decreased.

27. The method for regulating a write current for a magnetic memory cell of claim 25, wherein the magnitude of the magnetic memory cell write current is increased by incrementing an up/down counter.

28. The method for regulating a write current for a magnetic memory cell of claim 25, wherein the magnetic memory cell write current comprises an easy axis current and a hard axis current, the hard axis current being set to a default value, and the easy axis current being incremented.

29. The method for regulating a write current for a magnetic memory cell of claim 26, wherein the magnitude of the magnetic memory cell write current is decreased by decrementing an up/down counter.

30. The method for regulating a write current for a magnetic memory cell of claim 28, the up/down counter is connected to a current digital to analog converter (iDAC) that generates the magnetic memory cell write current.

31. The method for regulating a write current for a magnetic memory cell of claim 30, wherein the write current offset is subtracted from the magnetic memory cell write current by subtracting a current offset from a current reference of iDAC.

32. The method for regulating a write current for a magnetic memory cell of claim 31, wherein the current offset is subtracted from a current reference of iDAC by selecting which transistors of a plurality of transistor are connected in parallel in a current mirror, wherein the current mirror generates the current reference.

33. An apparatus for regulating a write current for a magnetic memory cell comprising:

a write current generator for generating a write current, the write current being magnetically coupled to the magnetic memory cell;

at least one test magnetic memory cell, the write current being magnetically coupled to the at least one test magnetic memory cell;

wherein the write current generator includes;

an up/down counter that controls a magnitude of the write current generated by an iDAC.

34. The apparatus for generating a write current of claim 33, wherein the write current generator further comprises a current mirror for providing a reference current to the iDAC.

35. The apparatus for generating a write current of claim 34, wherein the current mirror comprises a plurality of parallel transistors, wherein an offset current can be added to the reference current by selecting which of the plurality of transistors are conducting.

36. The apparatus for generating a write current of claim 34, wherein the write current being magnetically coupled to the at least one test magnetic memory cell comprises a continuous series of pulses, in which the pulses alternate in polarity.

37. The apparatus for generating a write current of claim 34, further comprising

a test magnetic memory cell state detector for detecting a logical state of the at least one test magnetic memory cell, an output of the test magnetic memory cell state detector being fed back to the write current generator.

38. The apparatus for generating a write current of claim 34, wherein the write current generator comprises an easy axis write current and a hard axis write current.

39. The apparatus for generating a write current of claim 34, wherein the write current is monitored over time.

40. The apparatus for generating a write current of claim 33, wherein the write current is re-calibrated upon detection of a predetermined variation in a temperature of the apparatus.

41. The apparatus for generating a write current of claim 33, wherein a negative offset current is added to the reference current, and if a write test to the at least one test magnetic memory cell fails, the up/down counter is incremented until the write test is passed.

42. The apparatus for generating a write current of claim 35, wherein a positive offset current is added to the reference current, and if a write test to the at least one test magnetic memory cell fails, the up/down counter is decremented until the write test is passed.

43. An array of magnetic memory cells, the array comprising an apparatus for generating a write current for writing to the magnetic memory cells, the apparatus comprising:

a write current generator for generating a write current, the write current being magnetically coupled to the magnetic memory cell;

at least one test magnetic memory cell, the write current being magnetically coupled to the at least one test magnetic memory cell; wherein

a switching response of the at least one test magnetic memory cell determines a magnitude of the write current generated by the write current generator;

wherein the write current generator includes;

an iDAC that generates the write current;

an up/down counter that controls the iDAC.

44. An apparatus for regulating a write current for a magnetic memory cell comprising:

means for modifying a magnetic memory cell write current by summing a write current offset to the magnetic memory cell write current;

means for determining whether writing to a magnetic memory cell with the modified magnetic memory cell write current results in a write error condition;

means for incrementing the magnetic memory cell write current, or decrementing the magnetic memory cell write current, until the write error condition is eliminated.